REMARKS

In the September 7, 2005 Written Opinion, the Authorized Officer objected to claims 1-52 under PCT Rule 66.2(a)(ii) and PCT Article 33 for alleged lack of novelty and/or inventive step over various cited references discussed in Item V of the Written Opinion. Specifically, the Authorized Officer objected:

claims 1, 3, 5, 7, 8, 10-12, 15, 16, 20, 21, 25, and 27 for alleged lack of novelty over D1;

claims 2, 6, 9, 17, 22-24, 26 and 28 for alleged lack of inventiveness over the combination of D1 and D2;

claim 13 for alleged lack of inventiveness over the combination of D1 and D3;

claim 4 for alleged lack of inventiveness over the combination of D1 and D4;

claim 14, 18, 19, and 29 for alleged lack of inventiveness over D1;

claims 30-48 for alleged lack of inventiveness over D5;

claim 49 for alleged lack of novelty over D2, D3, D4 and D7; and

claim 50-52 for alleged lack of novelty over D2.

In response, applicants have hereby deleted the original claims 20-29 and 49-52 and renumbered the original claims 30-48 as new claims 20-38. Further, applicants have amended the original claims 1 and 4 and the renumbered claims 20, 25, 28-31, and 35 (original claims 30, 35, 38-41, and 45).

Applicants respectfully traverse the lack of novelty and/or inventiveness objections raised by the Authorized Officer, due to the following patentable distinctions between the amended and/or renumbered claims 1-38 of the present invention and the cited references.

Patentable Distinctions Between Amended Claims 1-19 and D1-D7

Claim 1, from which claims 2-19 depend, has been hereby amended to recite:

"A process for fabricating a complementary metal oxide semiconductor (CMOS) structure comprising:

providing a plurality of polySi gates overlying a semiconductor substrate, each polySi gate comprises a dielectric cap located on an upper surface thereof;

forming silicided source/drain regions in the semiconductor substrate;

forming a patterned dielectric stack on the semiconductor substrate;

performing an etching process to selectively remove the dielectric cap against polySi and thereby expose an upper surface of each polySi gate, wherein the etching process does not etch the polySi gates, so that the exposed polySi gates formed by the etching process have substantially the same height; and

performing a salicide process which converts each polySi gate to a metal silicide gate, wherein each metal silicide gate has substantially the same height, is composed of the same silicide phase, and has substantially the same workfunction for the same polySi ion implant conditions."

Support for such claim amendments can be found in the specification at paragraph [0081].

The process recited by claims 1-19 of the present invention forms silicide source/drain regions before formation of metal silicide gates, by protecting the un-salidated polySi gates using dielectric caps during the source/drain salicidation process. More importantly, such a process removes the dielectric caps from the polySi gates after the source/drain salicidation, by using an etching process to selectively remove the dielectric cap but without etching the polySi gates, to form exposed polySi gates of substantially the same height for subsequent gate salicidation.

D1 discloses use of dielectric caps or salicide blocks 61 for protecting the polySi gate conductors 50 during source/drain salicidation (see Figure 7 of D1), and such dielectric caps 61 are subsequently removed from the gate conductors 50 to expose upper surfaces of the gate conductors 50 for gate salicidation (see Figure 8 of D1).

However, nothing in D1 teaches or suggests how the dielectric cap 61 is removed, much less the use of an etching process that selectively removes the dielectric caps 61 without etching the polySi gates 50. In fact, D1 teaches in paragraph [0017] "the complete removal of the salicide block 61 and the non-reacted amorphous silicon layer 58," suggesting that the process used for removing the dielectric cap 61 also removes the amorphous silicon and is therefore not selective. It is very likely that such a process will also remove a portion of the polySi gates 50, resulting in exposed polySi gates of various heights.

Therefore, D1 fails to provide any derivative basis for selective removal of the dielectric cap using an etching process that does not etch the polySi gates, as positively recited by claims 1-19 of the present application.

D2 discloses use of an etching process for exposing upper surfaces of polysilicon gates 126, 136 and 146 (see Figure 8 of D2), while such an etching process removes portions of the dielectric layers 310 and 320 as well as the polysilicon gates 126, 136 and 146 in a non-selective manner (see D2, column 5, lines 7-16). Therefore, D2 cannot remedy the deficiency of D1.

D3 does not even disclose the use of any dielectric cap for protecting the polysilicon gates G1 and G101 during the source/drain salicidation process. Instead, D3 only discloses polysilicon gates G1 and G101 that contain gate metal silicides GS1 and GS101 that have been formed together with the source/drain silicides DS1, DS101, S1, and S101 (see Figure 1 and the underlined section in the English translation of D3, which is enclosed herewith). Therefore, D3 cannot remedy the deficiency of D1.

D4 discloses metal gates 25, which are not deposited until after the source/drain salicidation process (see Figure 17 and column 6, lines 66-67 of D4). The dielectric caps 7b disclosed by D4 are located on top of protruding portions of the N well region 6 and the P well region 5 (see Figure 3 and column 3, lines 21-49 of D4), but **not** over polySi gates as positively recited by claims 1-19 of the present application.

Therefore, D4 fails to even disclose use of dielectric caps for protecting polySi gates during source/drain salicidation process, and it cannot remedy the deficiency of D1.

D5 discloses only tantalum silicide gate 20 that have already been formed before formation of the source/drain tantalum silicide contacts 32 (see Figures 4 and 10 of D5). Nothing in D5 teaches polySi gates, much less protection of polySi gates against source/drain salicidation by using dielectric caps. Therefore, D5 cannot remedy the deficiency of D1.

D6 discloses polySi gates 123 that are protected by dielectric caps 125 (see Figures 1-8 of D6). However, the dielectric caps 125 are not subsequently removed from the polySi gates 123 (see Figures 1-8 of D6). Therefore, D6 cannot remedy the deficiency of D1.

D7 discloses formation of gate metal silicide 62 over the polysilicon gates 30, while the source/drain regions are protected by masking layer 70 (see Figure 5 of D7). However, nothing in D7 teaches or suggests formation of source/drain metal silicide contacts, much less use of dielectric caps for protecting the polysilicon gates 30 during the source/drain salicidation process, or subsequent removal of such dielectric caps. Therefore, D7 cannot remedy the deficiency of D1.

In summary, claims 1-19 of the present application as amended herein patentably distinguish over the cited references D1-D7.

Patentable Distinctions Between Amended/Renumbered Claims 20-38 and D1-D7

The amended and renumbered claim 20, from which claims 21-28 depend, recites the step of "selectively removing silicide metal from atop each of the polySi gates by using an etching process to expose an upper surface of each of the polySi gates, wherein the etching process does not etch the polySi gates, so that the exposed polySi gates formed by the etching process have substantially the same height," followed by formation of silicide contact regions between each of the polySi gates (i.e., source/drain metal silicides). The amended and renumbered claim 29, from which claims 30-38 depend, correspondingly recites the step of "selectively removing the metal layer from atop each polySi gate by utilizing an etching process to expose an upper surface of each of the polySi gates, wherein the etching process does not etch the polySi gates, so that the polySi gates formed by the etching process have substantially the same height," followed by formation of silicide contact regions between each of the polySi gates (i.e., source/drain metal silicides).

Support for such claim amendments can be found in the specification at paragraphs [0096], [00105] and [00111].

The process recited by claims 20-38 of the present invention forms source/drain metal silicide contacts without salicizing the polySi gate, by **selectively removing the silicide metal from the un-salidated polySi gates prior to the source/drain salicidation process**. Further, the silicide metal is selectively removed, by using an etching process that does not etch the polySi gates, to form exposed polySi gates of substantially the same height.

D1-D4 do not, in any manner, teach or suggest selective removal of silicide metal or metal from polySi gates.

D5 discloses formation of a metal-silicide containing layer 32 atop gates 20 and subsequent removal of the metal-silicide layer 32 from the gates 20 (see Figures 8 and 10 and column 5, lines 34-65 of D5). However, claims 20 and 29, from which claims 21-28 and 29-38 depend, recites a silicide metal or a metal, **not** metal silicide. The silicide metal is a metal that is capable of forming metal silicide, but it is still a metal, not metal silicide.

Therefore, D5 does not, in any manner, teach or suggest selective removal of the silicide metal or metal, as recited by claims 20-38 of the present invention.

D6 discloses deposition of a silicide source metal layer 160 (see Figure 8 and paragraph [0049] of D6). However, source/drain salicidation process is carried out without removing any portion of the silicide source metal layer 160 (see paragraph [0050] of D6). Therefore, claims 20-38 of the present invention patentably distinguish over D6, by positively reciting selective removal of the silicide metal or metal from the polySi gates, followed by the source/drain salicidation

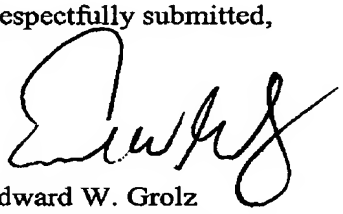
D7 does not, in any manner, teach or suggest selective removal of silicide metal or metal from polySi gates. Therefore, D7 cannot remedy the above-described deficiencies of D5 and D6.

In summary, claims 20-38 of the present application as amended and/or renumbered herein patentably distinguish over all the cited references D1-D7.

Based on the foregoing, it is clear that all claims 1-38 now pending in the present application fully comply with the novelty and inventiveness requirements of PCT Rule 66.2(a)(ii) and PCT Article 33.

It therefore is requested that the International Preliminary Examination Report for this application now be established, based on the claims 1-38 pending in the application following entry of the enclosed replacement claims pages 27-32.

Respectfully submitted,



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Attachments: Six (6) Substitute sheets of claims